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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ITSUO HIDAKA	:	
Appl. No.: 09/525,802	:	Art Unit: 2815
Filed: March 15, 2000	:	Examiner: CRUZ, L.
For: SEMICONDUCTOR DEVICE	:	Atty Docket: AKM-00301

CERTIFICATE OF MAILING

I hereby certify that the foregoing document is being deposited with the United States Postal Service as first class mail, postage prepaid, "Post Office to Addressee", in an envelope addressed to: Commissioner of Patents, Washington, DC 20231 on October 16, 2000.

Bonny Rogers

SUPPLEMENTAL AMENDMENT AND RESPONSE

Commissioner for Patents
Washington, D.C. 20231

Sir:

This paper is being provided in response to the Office Action dated June 21, 2000, for the above-captioned U.S. patent application and as a supplement to Applicant's response filed on September 12, 2000

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required for consideration of this paper (including fees for net addition of claims) are authorized to be charged in two originally-executed copies of an Amendment Transmittal Letter filed herewith.

Kindly enter the following amendments:

IN THE CLAIMS:

Please amend Claims 1-6, 8-10, 13, 17, and 18 as follows:

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1. (Twice Amended) A semiconductor device having multiple wiring layers, comprising:

B1 Cont'd

[a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers;]

Sub C

a signal line which is formed in a [one of said] wiring [layers] layer, and to which a signal voltage is applied;

two adjacent lines which are so [disposed] adjacent to said signal line [so] as not to be connected thereto, and which are formed in a [same one of said plurality of] wiring [layers] layer where said signal line is formed;

two intersection lines which are respectively formed in [different ones of said plurality of] wiring layers, each [of said intersection lines] being present [separated from said signal line] via an [one of said plurality of] insulating [layers] layer above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through the insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines and said two intersection lines.

wherein said signal line is completely enclosed by said two adjacent lines, said two intersection lines, and said entire-line-area through-holes, which are one of conductors and semiconductors.

B1 contd

2. (Twice Amended) The semiconductor device according to claim 1, wherein said two adjacent lines[, which are formed in said same one of said plurality of wiring layers where said signal line is formed,] are formed substantially in parallel to said signal line.

3. (Twice Amended) The semiconductor device according to claim 1, wherein electric potentials of said two adjacent lines [formed in the same wiring layer as said signal line], said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value. Int. Use

4. (Twice Amended) The semiconductor device according, to claim 1, wherein electric potentials of said two adjacent lines [formed in the same wiring layer as said signal line], said two intersection lines and said entire-line-area through-holes have a same phase as a phase of an electric potential of said signal line. Int. Use

5. (Twice Amended) A semiconductor device having multiple wiring layers, comprising:

[a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers;]

a plurality of signal lines which are formed not to intersect each other in an identical [one of said plurality of] wiring [layers] layer, and to which signal voltages having a same phase are applied;

two adjacent lines which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto, and which are formed in the [identical one of said plurality of] wiring [layers] layer where said plurality of signal lines are formed;

two intersection lines which are formed in a wiring layer each being present [separated from said signal lines] via [selected ones of said plurality of] insulating layers above or under the wiring layer where said plurality of signal lines and said two adjacent lines are formed, and which are formed along, a surface area corresponding to an area enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines with said two intersection lines.

wherein said plurality of signal lines are completely enclosed by said two adjacent lines, said two intersection lines, and said plurality of entire-line-area through-holes, which are one of conductors and semiconductors.

B1 could

6. (Twice Amended) The semiconductor device according to claim 5, wherein electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value.

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7. Int. use

B2 cont'd

8. (Twice Amended) A semiconductor device having multiple wiring layers, said device comprising:

[a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers;]

sub C3

a plurality of signal lines which are formed not to intersect each other in an identical [one of said plurality of] wiring [layers] layer, and to which signal voltage having different phases are applied; Intl. use

two first adjacent lines which are so formed adjacent respectively onto a selected outer two of said plurality of signal lines as not to be connected thereto, and which are formed in the [same one of said plurality of] wiring [layers] layer where said plurality of signal lines are formed;

at least one second adjacent line which is formed in the [same one of said plurality of] wiring [layers] layer where said plurality of signal lines are formed, between said plurality of signal lines so as not to be connected to said plurality of signal lines;

two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where said signal lines and said first adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by said two first adjacent lines; and

entire-line-area through-holes which respectively penetrate through insulating layers formed between said first and second adjacent lines and said two intersection lines along entire areas of said first and second adjacent lines, and which respectively and electrically connect said first and second adjacent lines with said two intersection lines, wherein said plurality of signal lines are completely enclosed by said two first adjacent lines, said at least one second adjacent line, said two intersection lines, and said entire-line-area through-holes, which are one of semiconductors and conductors.

9. (Twice Amended) The semiconductor device according to claim 8, wherein electric potentials of said first and second adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value.

10. (Twice Amended) A semiconductor device having multiple wiring layers, said device comprising:

B2 Cont'd

[a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers;]

a plurality of signal lines which are formed substantially in parallel to each other in different [ones of said plurality of] wiring layers, and to which signals having a same phase are respectively applied;

a plurality of adjacent lines, each pair of which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto in the wiring layers where said plurality of signal lines are formed;

two intersection lines, each of which is formed in a layer under a lowermost wiring layer where said plurality of signal lines are formed or in a layer above an uppermost wiring layer where said plurality of signal lines are formed, and which are formed along a surface area corresponding to an area enclosed by said plurality of adjacent lines formed on the both extreme sides of said plurality of signal lines;

a plurality of first entire-line-area through-holes which penetrate through an insulating layer arranged between said adjacent lines and said two intersection lines, along entire areas of said adjacent lines, and which electrically connect said adjacent lines with said two intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through an insulating layer arranged between said adjacent lines, along the entire areas of said adjacent lines, and which electrically connects said adjacent lines with each other.

wherein said plurality of signal lines are completely enclosed by said adjacent lines, said two intersection lines, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors.

11,12 → Int. use

13. (Twice Amended) A semiconductor device having multiple wiring layers, said device comprising:

[a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers;]

a plurality of signal lines which are formed in different [selected ones of said plurality of] wiring layers, and to which signal voltages are respectively applied;

a plurality of adjacent lines, each pair of which are formed either in a lowermost or uppermost wiring layer of the wiring layers where said plurality of signal lines are formed, respectively adjacent onto both sides of a selected one of said plurality of signal lines which is formed in an identical layer, thereby not to be connected to the selected one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a wiring layer under the lowermost wiring layer of said signal lines, or in a wiring layer above the uppermost wiring layer of said signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said plurality of signal lines formed either in the lowermost or uppermost wiring layer of said signal lines;

14 & 15 Int. use

16 → Rejection

B3 cont'd

a second intersection line which is formed in a wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection [lines] line, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection [lines] line,

wherein said plurality of signal lines are completely enclosed by said plurality of adjacent lines, said two first intersection lines, said second intersection line, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors.

17. (Twice Amended) A semiconductor device having a structure in which a [selected one] signal line [of a plurality of signal lines], to which a [selected] signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, whose electrical potentials are set at a predetermined value, wherein said signal line is completely enclosed by two adjacent lines, two intersection lines, and entire-line-area through-holes, which are one of conductors and semiconductor, said two adjacent lines being adjacent to said signal line and formed in a wiring layer where said signal line is formed, said two intersection lines being formed in a wiring layer above or under the wiring layer where said signal line and said adjacent lines are formed, said entire-line-area through-holes penetrating through insulating layers formed between said two adjacent lines and said two intersection lines and said two intersection lines along entire areas of the two adjacent lines.

18. (Twice Amended) A semiconductor device having a structure in which a [selected one] signal line [of a plurality of lines], to which a [selected] signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, to which a voltage whose electric potential has a same phase as a phase of said signal line is applied, wherein said signal line is completely enclosed by two adjacent lines, two intersection lines, and entire-line-area through-holes, which are one of conductors and semiconductor, said two adjacent lines being adjacent to said signal line and formed in a wiring layer where said signal line is formed, said two intersection lines being formed in a wiring layer above or under the wiring layer wherein said signal line and said adjacent lines are

B4 cancel

formed, said entire-line-area through-holes penetrating through insulating layers formed between said two adjacent lines and said two intersection lines and said two intersection lines along entire areas of the two adjacent lines.

REMARKS

This paper is being provided in response to the June 21, 2000 Office Action for the above-referenced application and as a supplement to Applicant's response filed on September 12, 2000. In this supplemental amendment and response, Applicant has amended Claims 1-6, 8-10, 13, 17, and 18 in order to more particularly point out and distinctly claim that which Applicant deems to be the invention. Applicant respectfully submits that the amendments to the claims are all supported by the originally filed application.

The rejection of Claims 1 - 4 under 35 U.S.C. §102(b) as being anticipated by Landis (U.S. Patent No. 4,673,904, hereinafter referred to as "Landis") is hereby traversed and reconsideration thereof is respectfully requested. Applicants respectfully submit that Claims 1 - 4, as amended herein, are patentably distinct over the cited reference.

Independent Claim 1, as amended herein, recites a semiconductor device having multiple wiring layers. A signal line is formed in a wiring layer to which a signal voltage is applied. Two adjacent lines are so adjacent to the signal line as not to be connected thereto, and which are formed in a layer where the signal line is formed. Two intersection lines are respectively formed in wiring layers each being present via an

insulating layer above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by the two adjacent lines. A plurality of entire-line-area through-holes respectively penetrate through the insulating layers formed between the adjacent lines and the two intersection lines, along entire areas of the two adjacent lines, and which respectively and electrically connect the two adjacent lines and the two intersection lines.

Claims 2-4 depend from Claim 1.

Landis relates to multilayered boards used for supporting and/or interconnecting various components of an electrical circuit, and more particularly to a method of making a board having a shielded conductor embedded therein. (Col. 1, Lines 5-10). Landis discloses a board that includes a metallic base and a layer of dielectric material. Imbedded in the dielectric layer are a plurality of conductors. Depending on the required degree of isolation, some of the conductors are completely shielded by tubular shields having a rectangular cross-section. These shields are formed on the copper base so that they are electrically connected to the ground plane. The remaining conductors are partially shielded by a U-shaped shield, or merely decoupled by the I-shaped isolating walls. (Col. 2, Lines 20-31; Figures 2 and 3). For terminating purposes the two extreme portions of each conductor have a vertical section 50 which ends in a square pad flush with the top surface 54 of the board, which then are wirebonded to the pads of the IC's 56 and 58 (Col. 2, Lines 32-47).

Applicant respectfully submits that the Landis neither discloses nor suggests a ***semiconductor device having multiple wiring layers wherein a signal line is completely enclosed by two adjacent lines, two intersection lines, and entire-line-area through-holes, which are one of conductors and semiconductors***, as set forth in Claim 1. Rather, as pointed out above, Landis discloses conductors having varying degrees of isolation and shielding in which the shielding disclosed uses tubular shields formed on a copper base so that they are electrically connected to the ground plane. There is no disclosure or suggestion in Landis of a structure of through-holes. Furthermore, Landis merely discloses the structures of the board and substrate without making mention of the wiring structure of the semiconductor.

In view of the foregoing, Landis neither discloses nor suggests Applicant's Claims 1-4, as amended herein. Accordingly, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 5 - 18 under 35 U.S.C. §102(b) as being anticipated by Schreiber et al (U.S. Patent No. 4,845,311, hereinafter referred to as "Schreiber") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 5 - 18, as amended herein, are patentably distinct over the cited reference, for the reasons set forth below.

Independent Claim 5, as amended herein, recites a semiconductor having multiple wiring layers. A plurality of signal lines are formed so as not to intersect each other in an

identical wiring layer, and to which signal voltages having a same phase are applied. Two adjacent lines are so formed adjacent onto both sides of the plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where the plurality of signal lines are formed. Two intersection lines are formed in a wiring layer each being present via insulating layers above or under the wiring layer where said plurality of signal lines and the two adjacent lines are formed, and which are formed along a surface area corresponding to an area enclosed by the two adjacent lines. A plurality of entire-line-area through-holes respectively penetrate through insulating layers formed between the adjacent lines and the two intersection lines, along entire areas of the two adjacent lines, and which respectively and electrically connect the two adjacent lines with the two intersection lines. The plurality of signal lines are completely enclosed by the two adjacent lines, the two intersection lines, and the plurality of entire-line-area through-holes, which are one of conductors and semiconductors. Claims 6 and 7 depend from Claim 5.

Independent Claim 8, as amended herein, recites a semiconductor device having multiple wiring layers. A plurality of signal lines are formed so as not to intersect each other in an identical wiring layer, and to which signal voltage having different phases are applied. Two first adjacent lines are so formed adjacent respectively onto a selected outer two of said plurality of signal lines as not to be connected thereto, which are formed in the wiring layer where the plurality of signal lines are formed. At least one second adjacent line is formed in the wiring layer where the plurality of signal lines are formed, between the plurality of signal lines so as not to be connected to the plurality of signal

lines. Two intersection lines are each formed in a wiring layer being present via an insulating layer above or under the wiring layer where the signal lines and the first adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by the first two adjacent lines. Entire-line-area through-holes respectively penetrate through insulating layers formed between the first and second adjacent lines and the two intersection lines along entire areas of the first and second adjacent lines, and which respectively and electrically connect the first and second adjacent lines with the two intersection lines. The plurality of signal lines are completely enclosed by the two first adjacent lines, the at least one second adjacent line, the two intersection lines, and the entire-line-area through-holes, which are one of conductors and semiconductors. Claim 9 depends from Claim 8.

Independent Claim 10, as amended herein, recites a semiconductor device having multiple wiring layers. A plurality of signal lines are formed substantially in parallel to each other in different wiring layers, and to which signals having a same phase are respectively applied. A plurality of adjacent lines are formed so that each pair which are so formed are adjacent onto both sides of the plurality of signal lines as not to be connected thereto in the wiring layers where the plurality of signals are formed. Two intersection lines are each formed in a layer under a lowermost wiring layer where the plurality of signals are formed or in a layer above an uppermost wiring layer where the plurality of signal lines are formed, and which are formed along a surface area corresponding to an area enclosed by the plurality of adjacent lines formed on the both extreme sides of the plurality of signal lines. A plurality of first entire-line-area through-

holes penetrate through an insulating layer arranged between the adjacent lines and the two intersection lines, along entire areas of the adjacent lines, and which electrically connect the adjacent lines with the two intersection lines. A plurality of second entire-line-area through-holes penetrate through an insulating layer arranged between the adjacent lines, along the entire areas of the adjacent lines, and which electrically connects the adjacent lines with each other. The plurality of signal lines are completely enclosed by the adjacent lines, the two intersection lines, the plurality of entire-line-area through-holes, and the plurality of second entire-line-area through-holes. Claims 11 and 12 depend from Claim 10.

Independent Claim 13, as amended herein, recites a semiconductor device having multiple wiring layers. A plurality of signal lines are formed in different wiring layers to which signal voltages are respectively applied. A plurality of adjacent lines are formed such that each pair are formed in either a lowermost or uppermost wiring layer of the wiring layers where the plurality of signal lines are formed, respectively adjacent onto both sides of a selected one of the plurality of signal lines which is formed in an identical layer, thereby not to be connected to the selected one of the plurality of signal lines. Two first intersection lines are formed each either in a wiring layer under the lowermost wiring layer of the signal lines, or in a wiring layer above the uppermost wiring layer of the signal lines, and each of which is formed along a surface area corresponding to an area enclosed by the pair of adjacent lines formed on the both sides of a corresponding one of the plurality of signal lines either in the lowermost or uppermost wiring layer of the signal lines. A second intersection line is formed in a wiring layer formed between

the wiring layers of the signal lines, and which is formed along a surface area corresponding to at least one area enclosed by the pair of adjacent lines. A plurality of first entire-line-area through-holes penetrate through insulating layers respectively formed between the adjacent lines and the first intersection lines, along entire areas of the adjacent lines, thereby electrically connecting the adjacent lines with the first two intersection lines. A plurality of second entire-line-area through-holes penetrate through insulating layers respectively formed between the adjacent lines and the second intersection line, along entire areas of the adjacent lines, thereby electrically connecting the adjacent lines with the second intersection line. The plurality of signal lines are completely enclosed by the plurality of adjacent lines, the first two intersection lines, the second intersection line, the plurality of first entire-line-area through-holes, and the plurality of second entire-line-area through-holes, which are one of conductors or semiconductors. Claims 14-16 depend from Claim 13.

Independent Claim 17, as amended herein, recites a semiconductor device having a structure in which a signal line, to which a signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, whose electrical potentials are set at a predetermined value, wherein said signal line is completely enclosed by two adjacent lines, two intersection lines, and entire-line-area through-holes, which are one of conductors and semiconductor, said two adjacent lines being adjacent to said signal line and formed in a wiring layer where said signal line is formed, said two intersection lines being formed in a wiring layer above or under the wiring layer where said signal line and said adjacent lines are formed, said entire-line-area through-holes penetrating through

insulating layers formed between said two adjacent lines and said two intersection lines and said two intersection lines along entire areas of the two adjacent lines.

Independent Claim 18, as amended herein, a semiconductor device having a structure in which a signal line, to which a signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, to which a voltage whose electric potential has a same phase as a phase of said signal line is applied, wherein said signal line is completely enclosed by two adjacent lines, two intersection lines, and entire-line-area through-holes, which are one of conductors and semiconductor, said two adjacent lines being adjacent to said signal line and formed in a wiring layer where said signal line is formed, said two intersection lines being formed in a wiring layer above or under the wiring layer wherein said signal line and said adjacent lines are formed, said entire-line-area through-holes penetrating through insulating layers formed between said two adjacent lines and said two intersection lines and said two intersection lines along entire areas of the two adjacent lines.

Schreiber relates generally to signal transmission lines, and more specifically, to flexible coaxial cables capable of transmitting signals in the GHz frequency range without appreciable signal loss and providing high density packaging. (Col. 1, Lines 6-12). The flexible cable includes one or more coaxial cables each of which include a central conducting signal line surrounded by a first dielectric layer. The signal return line is surrounded by a second dielectric layer which is in turn surrounded by a shield. (Col. 2,

Lines 18-34). The shield includes a plurality of electrically connected conductor elements. The bottom planar conductor elements is electrically connected through a first vertical conductor element to a signal trace. Continuity between a top planar conductor element and the signal trace is established by a second vertical conductor element. The top planar conductor element is electrically connected to the signal trace by a third vertical conductor element. The signal trace is electrically connected to the bottom planar conductor element by a fourth vertical conductor element thereby completing a substantially rectangular shield structure. (Col. 2, Lines 48-61). Each shield shares a common, substantially vertical conductor was with the neighboring shield, thereby joining together each adjacent coaxial structure. (Col. 2, Line 68-Col. 3, Line 3).

Applicant respectfully submits that Schreiber neither discloses nor suggests a ***semiconductor device having multiple wiring layers wherein a signal line is completely enclosed by two adjacent lines, two intersection lines, and entire-line-area through-holes, which are one of conductors and semiconductors***, as set forth in independent Claim 5. Rather, as discussed above, Schreiber discloses a flexible coaxial cable arrangement that includes a substantially rectangular shield structure comprised of a plurality of electrically connected conductor elements. Schreiber makes no mention or suggestion of internal wiring structure of a semiconductor chip.

Accordingly, Schreiber neither discloses nor suggests Applicant's Claim 5, as amended herein.

Applicant's independent Claims 8, 10, 13, 17, and 18 are also neither disclosed nor suggested by Schreiber in that Schreiber neither discloses nor suggests a ***semiconductor device having multiple wiring layers wherein a signal line is completely enclosed by two adjacent lines, two intersection lines, and entire-line-area through-holes, which are one of conductors and semiconductors***, as set forth in Applicant's Claims 8, 10, 13, 17, and 18.

In view of the foregoing, Applicant respectfully submits that Schreiber does not anticipate Claims 5-18 since Schreiber does not contain each and every feature of the claimed invention. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-951-6676.

Respectfully submitted,
HUTCHINS, WHEELER & DITTMAR

Date: October 16, 2000

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